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(54) Method of forming silicon oxynitride films on silicon substrates.

(57) The inventive method relates to the formation of a thin film of silicon oxynitride exhibiting a high breakdown voltage on a silicon substrate of a first conductivity type and comprises the steps of:

forming a thin film of silicon oxynitride on the silicon substrate;

forming a region of a second conductivity type in at least part of the silicon substrate by ion implantation through said thin film of silicon oxynitride; and

annealing said silicon oxynitride film in a wet O_2 ambient at a temperature between 700°C and 1000°C.

Preferably the deposited layer is annealed additionally after the deposition and prior to the ion implantation.

The method is applied in the formation of capacitor structures, like high capacitance storage capacitors for dynamic random access memory cells.

EP 0 260 473 A1

METHOD OF FORMING SILICON OXYNITRIDE FILMS ON SILICON SUBSTRATES

The present invention generally relates to a method of forming silicon oxynitride thin films on silicon substrates of a first conductivity type.

Thin film insulators are key materials in semiconductor integrated circuits, particularly in regard to their application as storage node dielectrics for the storage capacitor of the so-called "one device" dynamic random access memory (DRAM) cell. Typically, a thin film dielectric is thermally grown or deposited on a silicon wafer, and then a metal or polysilicon electrode is deposited on top of the thin film to form the charge plate of the capacitor.

Until recently, silicon dioxide (SiO_2) films have been the most widely used dielectric films due to the stable SiO_2/Si interface and the good insulating properties of SiO_2 films. However, the dielectric constant of SiO_2 is only 3.9. In present day dynamic random access memory cells wherein the thicknesses of the dielectric film is in the 10-15 nanometer (nm) range, a high yield and reliable SiO_2 film is difficult to grow. Moreover, the defect density of thin SiO_2 films within this thickness range also requires very tight control over a host of sensitive process conditions. More recently, silicon nitride (Si_3N_4) films have been utilized as storage node dielectrics. Si_3N_4 has a dielectric constant of 7, which is significantly higher than SiO_2. As such, a thicker layer may be used to improve yield and to reduce process sensitivity. Unfortunately, the d.c. leakage of Si_3N_4 is much higher than that of SiO_2. Moreover, Si_3N_4 films may produce film stresses of sufficient magnitude to generate crystal lattice dislocations in the underlaying silicon substrate.

Zimmer in U.S. Patent number 4,140,548 discloses a method of making a metal oxide semiconductor (MOS) which utilizes a two layer oxide. One of the layers is thermal SiO_2 and the other layer is deposited SiO_2. The very thin layer of thermal SiO_2 is formed by heating a silicon wafer in dry O_2 at 950°C.

Barile et al in U.S. Patent number 3,793,090 disclose an example of a composite of silicon dioxide-silicon nitride film used as the gate dielectric of a field effect transistor (FET). The composite film is annealed in dry oxygen at a temperature of 1050°C. In the Barile et al process a thin layer of silicon oxynitride forms on top of the nitride layer should the O_2 anneal be carried out prior to depositing the gate electrode.

U.S. Patent number 4,543,707 to Ito et al shows plasma chemical vapor deposited silicon oxynitride used as an electrode dielectric. Ito et al disclose that silicon oxynitride acts as a strong barrier against contaminants such as water, alkali ions, and other impurities. Ito et al also state that because of the high dielectric constant of silicon oxynitride, a high field threshold voltage can be obtained. The patent is generally related to stacking silicon oxynitride layers of different compositions on top of one another by varying the N/O ratio. The stacked silicon oxynitride layers tend to etch at different rates.

U.S. Patent 3,886,000 by Bratter et al discloses a semiconductor device in which silicon oxynitride is deposited by the reaction of carbon dioxide, ammonia, and silane. In this patent the silicon oxynitride is thermally oxidized to SiO_2.

Many patents have been issued relating to annealing processes that overcome various difficulties encountered in processing semiconductor films. An "anneal" is a heating process which drives out impurities from an exposed film, introduces elements that are present in the anneal ambient into the film, and densifies the film. U.S. Patent 4,001,049 to Baglin et al discloses a particular ion radiation treatment of amorphous SiO_2 film with a subsequent annealing procedure which improves the dielectric breakdown property of the film. The temperature range for annealing is from 200°C to 800°C. U.S. Patent 4,364,779 to Kamgar et al discloses a double annealing step for radiation hardening. U.S. Patent 4,397,695 to Arit et al discloses a method for stabilizing the current gain of NPN-Silicon transistors which includes two separate annealing processes at different temperatures. U.S. Patent 4,329,773 to Geipel, Jr. et al discloses a process in which a wet oxygen (steam) anneal is carried out on a substrate having implanted arsenic ions. Little or no alteration of the arsenic (As^+) concentration profile occurs when the anneal is carried out between the temperatures of 850°C and 1000°C. Burkhardt et al in IBM Technical Disclosure Bulletin, Vol. 18, No. 3, August 1975, page 753, disclose a post oxidation anneal procedure using a radio frequency (RF) heated susceptor which reduces mobile ion charge levels. Gardner in IBM Technical Disclosure Bulletin, Vol. 17, No. 1, June 1974, page 117, discloses a field-effect transistor gate annealing to reduce fixed charges in an SiO_2 layer.

P. H. Pan, J. Abernathy, and C. Schaeffer showed in an article appearing in The Journal of Electronic Materials, Vol. 14, No. 5, Sept. 1985, pages 617 to 632, that silicon oxynitride films deposited by LPCVD techniques are dominated by a mixed matrix of silicon, nitrogen, and oxygen, which may be expressed as (Si_x-O_y-N_z). The silicon oxynitride films were deposited in a hot wall LPCVD reactor at 800°C. The reactant gases were

(SiH_2Cl_2), ammonia (NH_3), and nitrous oxide (N_2O). The total deposition pressure was 0.4 mbar (0.3 Torr). Samples with refractive indices (n) ranging from 1.65 to 1.85 were obtained by varying the $N_2O/(N_2O + NH_3)$ gas ratio from 0.1 to 0.5. The film composition and structure of the LPCVD silicon oxynitride film was analyzed using Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS), and infrared techniques. Thermal SiO_2 and LPCVD Si_3N_4 films were used as a standard to determine the concentration of O, N, and Si. The Auger depth profile results indicated good compositional uniformity as a function of depth. The XPS peak for silicon oxynitride (103.1 eV) was between the peaks for SiO_2 (104 eV) and Si_3N_4 - (102.7 eV). Fourier transform infrared (FTIR) spectra indicated a broad Si-O-N stretching bond between 1080 cm^{-1} and 840 cm^{-1}. High frequency (1MHz) and quasi-static capacitor-voltage (C-V) measurements were used to determine the flatband voltage and surface state density. The breakdown voltage was defined as the voltage across an insulator when a current level of 10 A is conducted through the film. It was found that the average breakdown strength (i.e., the breakdown voltage divided by the film thickness) of the film as deposited (i.e., prior to any further processing such as implantation) was greater than 12 MV/cm and the deviation was less than 2 MV/cm. The conduction of these films before and after annealing (900°C in N_2 or O_2) was also discussed. The anneal cycle was found to reduce the positive charge and leakage currents in the oxynitride film.

In general, there is no teaching in the prior art of an anneal process that would materially improve the breakdown voltage of silicon oxynitride films after they have been processed for application as a storage node dielectric.

It is therefore an object of this invention to provide a method of overcoming the low voltage breakdown difficulties of silicon oxynitride for use as a storage node dielectric.

It is another object of this invention to provide a unique annealing process which decreases the propensity of low voltage breakdown in LPCVD silicon oxynitride films.

It is another object of the invention to provide a method of making a high quality insulating film which may be used in transfer gates and storage capacitors in dynamic random access memory cells.

These objects are achieved by methods as disclosed in claims 1 to 3.

According to the present invention, a unique annealing process materially improves the yield and breakdown voltage of silicon oxynitride films. More particularly the processes of the present invention allow to form a high yield and reliable storage node when a low pressure chemical vapor deposited (LPCVD) silicon oxynitride dielectric film is used as a storage capacitor. Thin films of silicon oxynitride are deposited by LPCVD onto a silicon substrate at a relatively low temperature over a short period of time. The ion implantation through the oxynitride film enhances the capacitance of the resulting storage node. The anneal process after the ion implantantion occurs just prior to electrode deposition of either polysilicon or metal. It has been found that this combination of steps results in silicon oxynitride films having particularly tight breakdown distribution and high breakdown voltages. These high yield and high breakdown voltages make LPCVD silicon oxynitride films more feasible as a dielectric for a storage node of a dense dynamic random access memory.

Preferably after deposition the film is annealed to reduce the positive charge accumulated during deposition while also densifying the film.

Preferably the silicon oxynitride film or layer is made less than approximately 15 nm in thickness. Films of this thickness formed according to the inventive methods have a refractive index between 1.65 and 1.85.

Other advantageous embodiments of the inventive methods are disclosed in the subclaims.

The foregoing and other objects, aspects and advantages of the invention will be better understood from the following detailed description of the preferred embodiments of the invention with reference to the accompanying drawings, in which:

Figures 1a-1d are graphs showing the breakdown distribution of a silicon oxynitride film (~8nm) deposited by LPCVD and brush cleaned, with a polysilicon electrode disposed on its upper surface;

Figures 2a-2d are graphs showing the breakdown distribution of a silicon oxynitride film (~8nm) deposited by LPCVD, brush cleaned, and N_2 annealed, with a polysilicon electrode disposed on its upper surface;

Figures 3a-3d are graphs showing the breakdown distribution of a silicon oxynitride film (~8nm) deposited by LPCVD, brush cleaned, and wet O_2 annealed, with a polysilicon electrode disposed on its upper surface;

Figures 4a-4d are graphs showing the breakdown distribution of a silicon oxynitride film (~12nm) deposited by LPCVD, wet O_2 annealed, bombarded with As^+ ions implanted into the silicon wafer, ash cleaned, brush cleaned, and N_2 annealed, with an aluminum electrode disposed on its upper surface;

Figures 5a-5d are graphs showing the breakdown distribution of a silicon oxynitride film (~12nm) deposited by LPCVD, N_2 annealed, bombarded with As^+ ions implanted into the silicon

wafer, ash cleaned, brush cleaned, and N_2 annealed, with an aluminum electrode disposed on its upper surface;

Figures 6a-6d are graphs showing the breakdown distribution of a silicon oxynitride film (~12nm) deposited by LPCVD, N_2 annealed, bombarded with As^+ ions implanted into the silicon wafer, ash cleaned, brush cleaned, and wet O_2 annealed, with an aluminum electrode disposed on its upper surface; and

Figures 7a-7d are graphs showing the breakdown distribution of a silicon oxynitride film (~12nm) deposited by LPCVD, wet O_2 annealed, bombarded with As^+ ions implanted into the silicon wafer, ash cleaned, brush cleaned, and wet O_2 annealed, with an aluminum electrode disposed on its upper surface.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

There will now be described a high yield process for creating a silicon oxynitride dielectric layer having a high breakdown voltage for storage capacitor applications.

The following process was carried out on a clean <100> P-type silicon wafer substrate. The silicon oxynitride is deposited on the substrate by LPCVD techniques to form a thin dielectric layer (H≤15 nm). The film is deposited in a hot-walled LPCVD reactor by reacting SiH_2Cl_2 (25 sccm), NH_3 (20 sccm), and N_2O (60 sccm) at a pressure of 0,47 mbar (0.35 Torr) and a temperature between 700°C and 900°C. Particularly good results have been obtained at a deposition temperature of 820°C. The refractive index of the resulting silicon oxynitride film is in the order of 1.65 to 1.85. Using the specific conditions noted above, the resulting refractive index is 1.755. The deposition rate is approximately 1.5 nm/min. The resulting silicon oxynitride matrix is of good compositional uniformity with respect to depth.

The above-described silicon oxynitride film was then processed in several different ways in an attempt to discern which method produced the highest yield and breakdown voltage. Referring to the drawings, the figures show the breakdown distribution resulting from these various processes. For each process, two different lots of wafers were processed and tested. Each lot consisted of eight wafers; each wafer had eight test sites that were individually monitored. The graphs show the number of test sites that exhibited breakdown at given voltages, for two sequential stress tests. For the first stress test (indicated in the figures as "1st Pass"), a voltage of 0-20 volts was applied to each test site to determine the initial yield. As shown in the graphs, "breakdown voltage" is defined as the applied voltage at which a current of 10 μA flows through the film. For example, test sites that exhibited a breakdown voltage of 0 to 3 volts conducted more current than the 10 μA threshold at a voltage of ≤ 3 volts (i.e., they were effective short circuits). For the second stress test (indicated in the figures as "2nd Pass"), the same 0-20 volt test voltage was applied to each test site. More test sites failed at the second pass than at first pass because the stress tests themselves cause those devices on the brink of failure to fail. For example, Figure 1a shows the results of a first silicon oxynitride process, in which after the first stress test, twenty-seven of the sixty-four test sites on the first lot of wafers had a breakdown voltage of ≤3 volts. Figure 1d shows the results of the first silicon oxynitride process, in which after the second stress test, forty-four of the sixty-four tests sites on the second lot of wafers had a breakdown voltage of ≤ 3 volts.

Figures 1a to 1d show the results of a process in which silicon oxynitride was deposited as described above, and then brush cleaned for one minute. A polysilicon electrode was then formed over the silicon oxynitride. Note that no anneal cycle has been carried out. As shown in Figure 1a, in the first lot of wafers only twenty percent of the test sites had a breakdown voltage of 10 volts when subjected to the first pass stress test (hereinafter referred to as "first pass"). More than fifty percent of the test sites had a breakdown voltage of less than 5 volts at first pass. After the second pass stress test (hereinafter referred to as "second pass"), about eighty percent of the test sites had breakdown voltages of three volts or less. While for some reason the second lot of wafers exhibited better breakdown characteristics at first pass (Figure 1c) than did the first lot at first pass (Figure 1a), the second pass results of the two lots are roughly consistent.

To remove the positive charge that may accumulate during deposition while increasing the density of the deposited film, an anneal may be performed in dry nitrogen or wet oxygen. In general, the N_2 anneal is performed in a gas flow of 20 liters/min. of N_2 at a temperature between 800°C and 1000°C. In general, the wet O_2 anneal is performed in a 5 liter/min. gas flow of dry O_2 with 7 cc of H_2O at a temperature between 700°C and 1000°C. Both anneal cycles are performed by conveying the wafers through an anneal chamber at a rate of four inches/min. (the wafers are five inches in diameter).

Figures 2a to 2d show the results of a process wherein again a layer of silicon oxynitride is deposited on a substrate and then brush cleaned before further processing. The structure was then annealed in nitrogen at 1000°C, and a polysilicon

electrode was formed over the silicon oxynitride. Upon comparing Figure 2a with Figure 1a it is apparent that at first pass the breakdown voltage is indeed improved. However, note that at second pass approximately sixty-nine percent of the test sites had a breakdown voltage of three volts or less, which is exactly the same result as was produced without an anneal cycle.

Figures 3a to 3d show the results of a silicon oxynitride process which is exactly the same as the above process, except an anneal in wet O_2 at 800°C was substituted for the N_2 anneal. Upon comparison of Figures 3a to 3d with Figures 2a to 2d it is apparent that the wet O_2 anneal produced results markedly better than those obtained using the N_2 anneal. For both lots, substantially all of the test sites exhibited a breakdown voltage of ten volts at both first and second pass.

For some device applications, an insulating film on silicon substrate is enough to form a storage node. However, most current high density memory cells utilize a "high capacitance" or "Hi-C" storage node, in which a thin N-type layer is implanted below the insulating layer to provide a PN junction whose junction capacitance enhances the total capacitance of the storage node. Moreover, the implant region provides greater immunity to soft errors. Note that the N-type implant is given by way of example; a P-type implant could also be used. An example of a Hi-C storage node is shown in an article by Klepner, IBM Technical Disclosure Bulletin, Vol. 19, No. 2, July 1976, pages 458-459.

To form the N-type region beneath the silicon oxynitride, As^+ ion implantation is performed to achieve a concentration of 10^{19} ions/cm^2. In the prior art, it was shown in the above referenced Geipel patent that a wet O_2 anneal does not alter the As profile. The ion implantation procedure contaminates the wafer and silicon oxynitride film (with e.g., carbon). Before an electrode may be deposited on the silicon oxynitride film the contamination should be removed by cleaning. The cleaning step may be performed by brush cleaning or ash cleaning. The film is brushed for one minute, or ash cleaned by exposure to an O_2 atmosphere at a pressure of 1.13 mbar (.85 Torr) at a power of 400 Watts for six minutes at room temperature. Other appropriate means of cleaning may be employed.

According to the invention, the silicon oxynitride dielectric film is annealed after the above implantation and cleaning steps. This annealing process occurs immediately prior to electrode deposition, and is the critical step in the manufacture of reliable high-capacitance silicon oxynitride storage capacitors.

Experiments were conducted wherein the silicon oxynitride was deposited, and annealed in an N_2 ambient or wet O_2 ambient. Then As^+ ions were implanted through the silicon oxynitride to the underlaying silicon, without a subsequent anneal. The vast majority of test sites exhibited a breakdown voltage of less than 5 volts.

Figures 4 to 7 show the results of processes in which a double anneal was utilized. The first anneal was carried out after the silicon oxynitride was deposited, and the second anneal was carried out after arsenic ion implantation. Figures 4a to 4d show the results where the first anneal was carried out in wet O_2 and the second anneal was carried out in an N_2 ambient. Note how in both first and second passes, a little less than fifty percent of the test sites exhibited a breakdown voltage of 15 volts, which is a full five volts greater than the breakdown distribution in Figures 1 through 3. This is because in Figures 4 through 7 a 12 nm layer of silicon oxynitride was formed, instead of the 8 nm layer as in Figures 1 through 3. However, note that upon second pass approximately fifty percent of the test sites exhibited a breakdown voltage of 1 volt or less. Figures 5a-5d show the results where both anneals were carried out in an N_2 ambient. Note that approximately sixty six percent of the test sites exhibit a breakdown voltage of 15 volts, with only approximately twenty five percent of the test sites exhibiting a breakdown voltage of one volt or less.

Figures 6 to 7 show the results when either N_2 or wet O_2 is used as the first anneal and wet O_2 is used as the second anneal. For both Figure 6 (first anneal in N_2) and Figure 7 (first anneal in wet O_2), note that none of the test sites have breakdown voltages of less than 10 volts at first pass. For both, the breakdown voltage after second pass for more than ninety percent of the test sites was 15-16 volts.

Additional experiments were carried out to optimize the temperature ranges for the processes shown in Figures 6 and 7. For the process shown in Figure 6 the N_2 anneal temperature was kept at 1000° C and the wet O_2 anneal was carried out at 600°C to 1000°C in 100°C increments. For all runs, acceptable results were achieved at first pass. However, at 600°C and 700°C, the breakdown voltages substantially declined at second pass. At 1000°C, the second pass yield was uniformally low. However, at 800°C the second pass results were outstanding (these results are shown in Figure 6). For the process shown in Figure 7, the first wet O_2 anneal temperature was varied at 800°C, 900°C, and 1000°C, with the second wet O_2 anneal temperature held at 800°C. The results indicate the 800°C range produced the best results (as shown in Figure 7).

Therefore, we have established that an anneal carried out between 700°C and 1000°C in a wet O_2 ambient after As^+ ion implantation through the oxynitride layer and right before the deposition of an electrode will materially enhance the breakdown voltage of capacitors that incorporate a silicon oxynitride layer as the storage node dielectric. Typically, one would not expect the choice of wet O_2 anneal versus an N_2 anneal to have such a profound effect upon the breakdown distribution of a silicon oxynitride layer, in that the wet O_2 anneal provides silicon and oxygen which may reduce the dielectric constant of silicon oxynitride toward that of stoichiometric silicon dioxide.

While the invention has been described in terms of the preferred embodiments which incorporate a one or a two step annealing, where the critical annealing is performed in wet O_2, those skilled in the art will recognize that the specific steps and parameters may be varied in the practice of the invention within the spirit and scope of the appended claims.

Claims

1. A method of forming a thin film of silicon oxynitride exhibiting a high breakdown voltage on a silicon substrate of a first conductivity type, comprising the steps of:

forming a thin film of silicon oxynitride on a silicon substrate;

forming a region of a second conductivity type in at least part of the silicon substrate by ion implantation through said thin film of silicon oxynitride; and

annealing said silicon oxynitride film in a wet O_2 ambient at a temperature between 700°C and 1000°C.

2. A method of forming a capacitor structure on the surface of a semiconductor substrate of a first conductivity type, comprising the steps of:

depositing a thin layer or film of silicon oxynitride on the substrate by use of a low pressure chemical vapor deposition process;

implanting dopant ions of a second conductivity type through said layer of silicon oxynitride to form an implanted region the substrate;

annealing said layer of silicon oxynitride, said second anneal being carried out in a wet O_2 ambient at a temperature between 700°C and 1000°C; and
forming an electrode on said layer of silicon oxynitride.

3. A method of forming a high capacitance storage capacitor for a dynamic random access memory cell formed on a semiconductor substrate of a first conductivity type, comprising the steps of:

forming a thin layer or film of silicon oxynitride on the substrate by the use of a low pressure chemical vapor deposition technique;

implanting ions of a second conductivity type through said thin silicon oxynitride layer into a surface portion of the substrate;

annealing said silicon oxynitride layer in a wet O_2 ambient at a temperature of between 800°C and 1000°C, and

forming an electrode on said thin layer of silicon oxynitride.

4. Method according to any one of claims 1 to 3, wherein a first annealing step is performed after depositing the thin film of silicon oxynitride but before the step of forming said region of said second conductivity type in the substrate.

5. Method according to claim 4, wherein said first annealing step is performed in an N_2 ambient at a temperature between 800°C and 1000°C, preferably above 800°C and below 1000°C or in an O_2 ambient at a temperature between 700°C and 1000°C, preferably about 700°C and below 1000°C and most preferred at about 800°C.

6. Method according to claim 4, wherein said first annealing step is carried out in an N_2 ambient at a temperature of 1000°C.

7. Method according to any one of claims 1 to 6, wherein the anneal after said ion implantation is performed at a temperature above 700°C and below 1000°C and most preferred at about 800°C.

8. Method according to any one of claims 1 to 7, wherein the substrate is a P-type silicon wafer substrate and wherein As-ions are implanted.

9. Method according to any one of claims 1 to 8, wherein after the ion implantation the then present structure is ash cleaned and/or brush cleaned.

10. Method according to any one of claims 1 to 9, wherein said electrode is comprised of polysilicon.

11. Method according to any one of claims 1 to 10, wherein said layer of silicon oxynitride is made less than approximately 15 nm in thickness.

FIG.1A
LOT #1, 1ST PASS

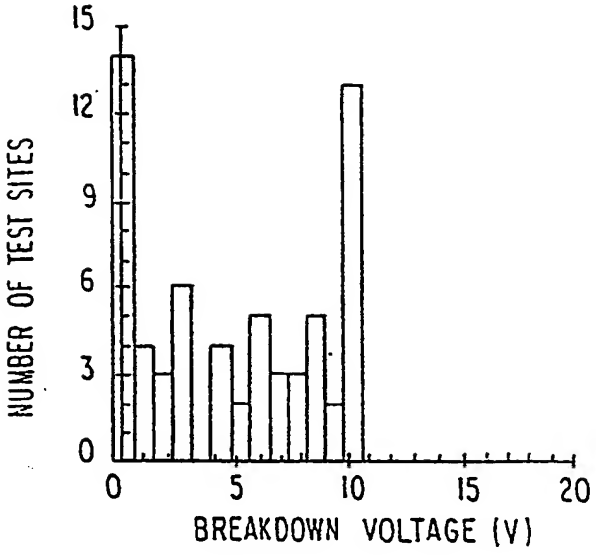
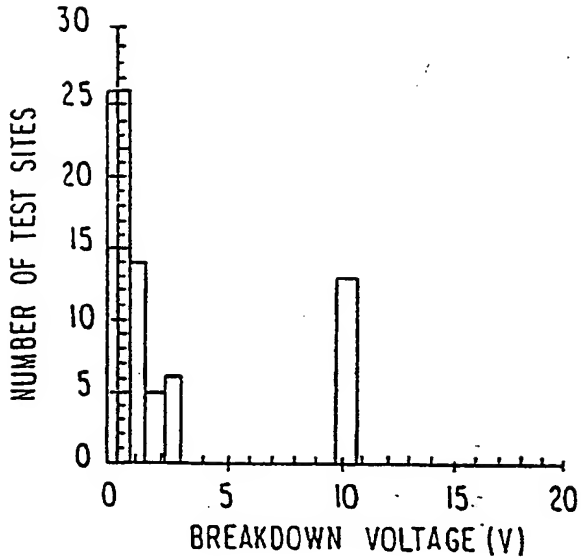


FIG.1B
LOT #1, 2ND PASS



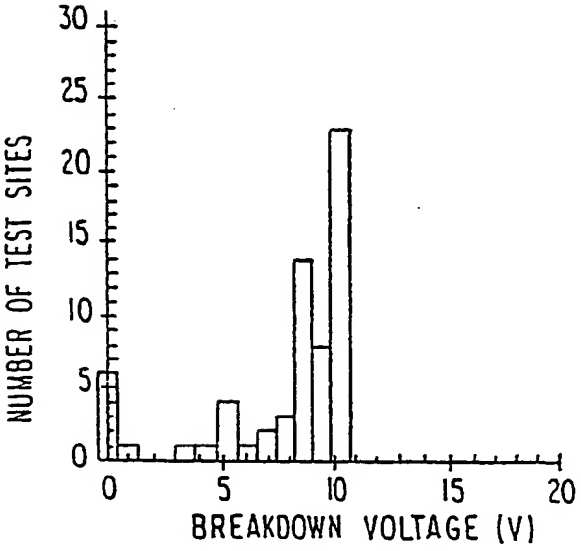


FIG.1C
LOT #2, 1ST PASS

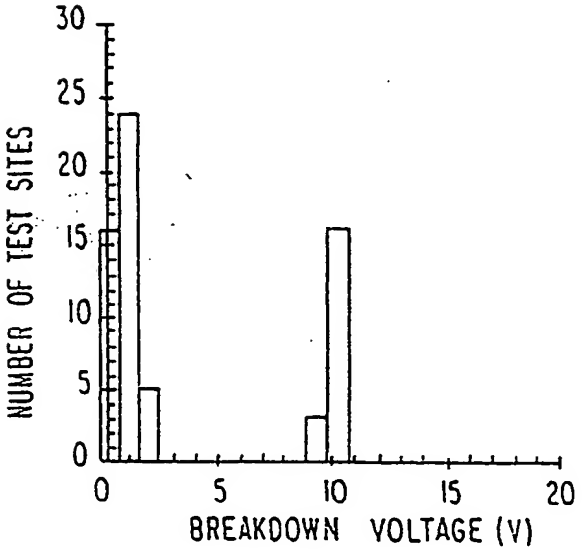


FIG.1D
LOT #2, 2ND PASS

FIG.2A
LOT # 1, 1ST PASS

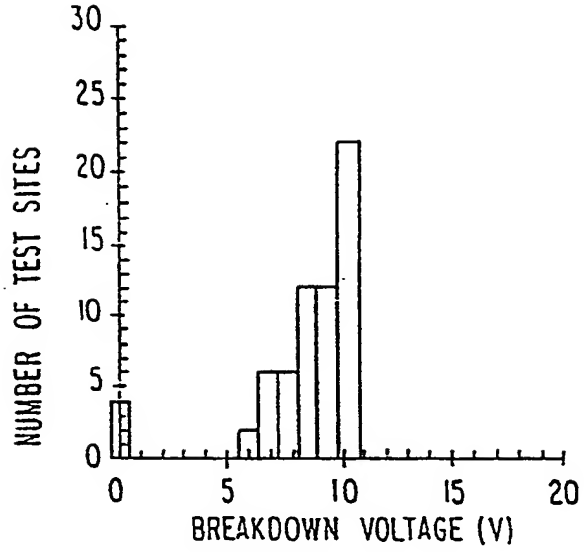
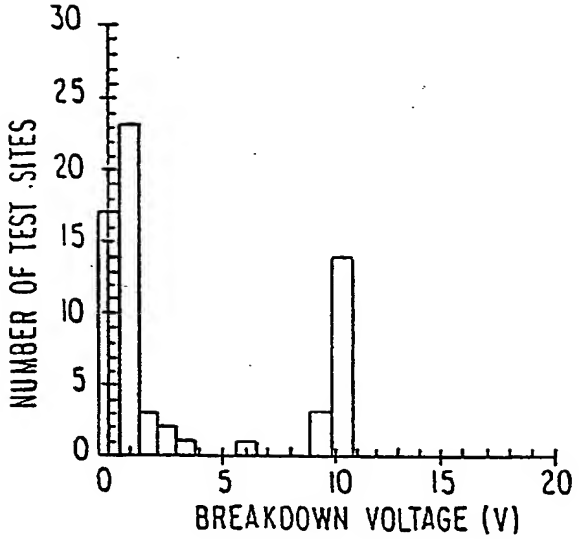


FIG.2B
LOT # 1, 2ND PASS



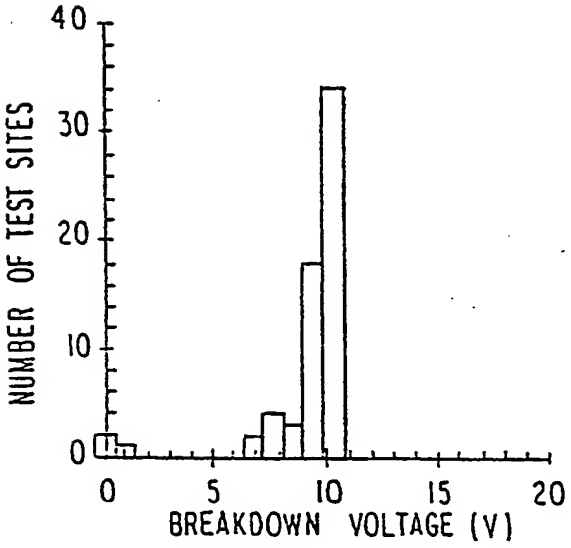


FIG.2C
LOT # 2, 1ST PASS

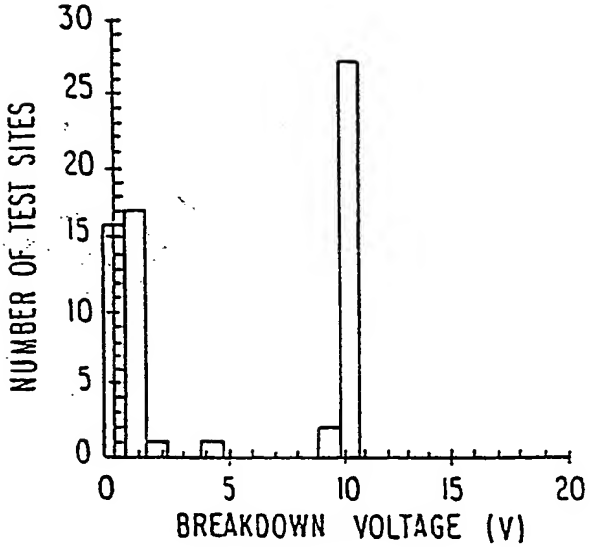


FIG.2D
LOT # 2, 2ND PASS

FIG.3A
LOT # 1, 1ST PASS

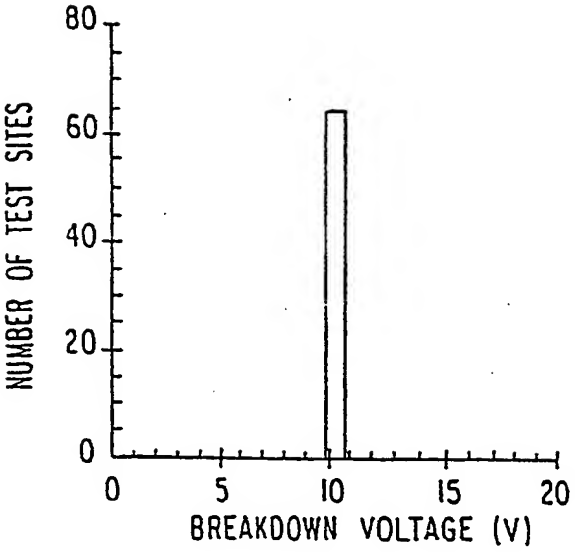
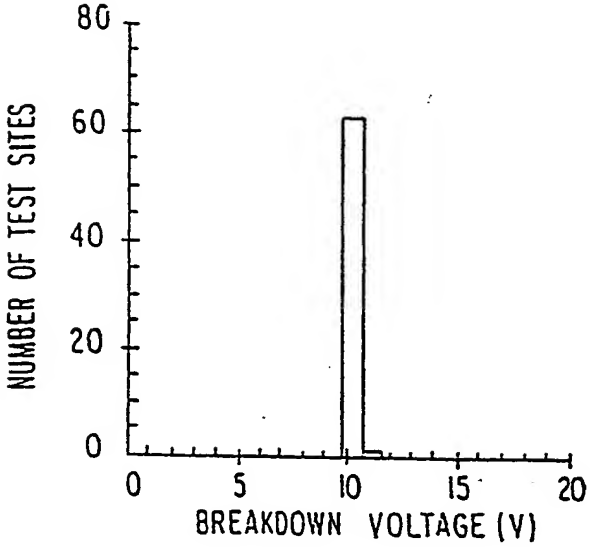


FIG.3B
LOT # 1, 2ND PASS



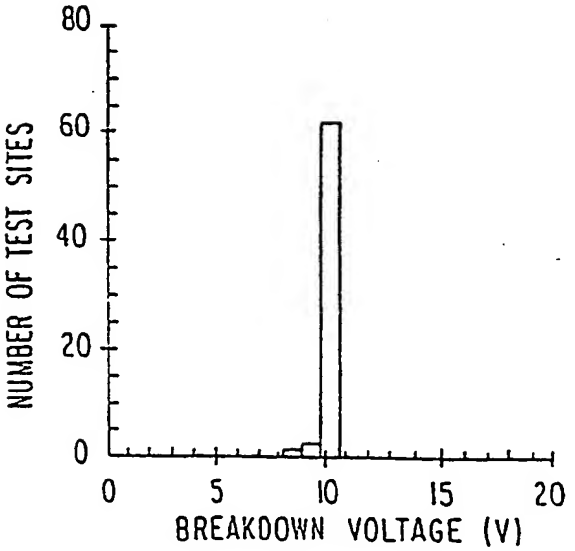


FIG.3C
LOT # 2, 1ST PASS

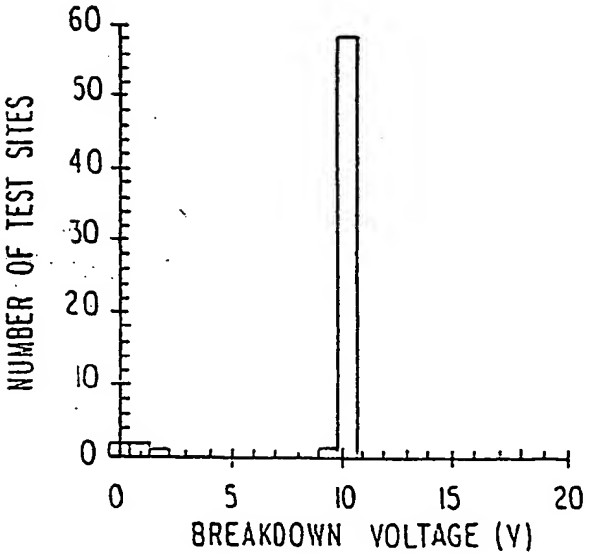


FIG.3D
LOT # 2, 2ND PASS

FIG. 4A
LOT #1, 1ST PASS

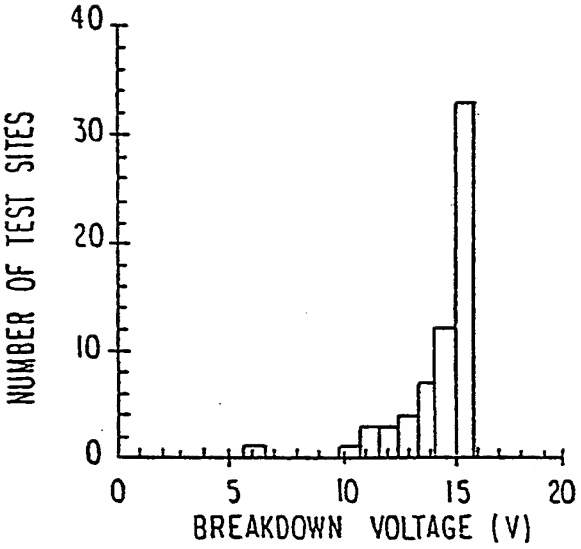
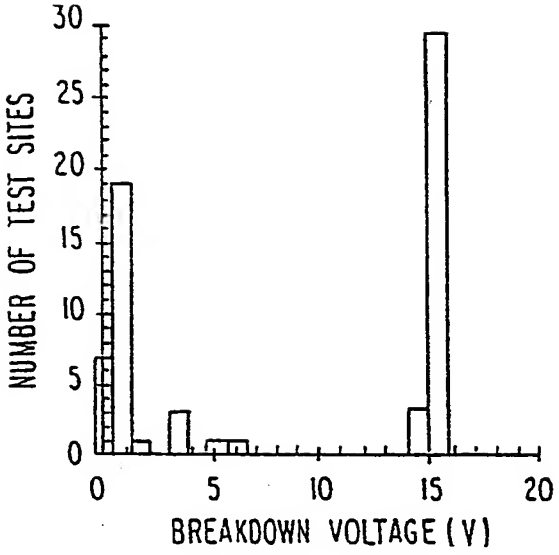


FIG. 4B
LOT # 1, 2ND PASS



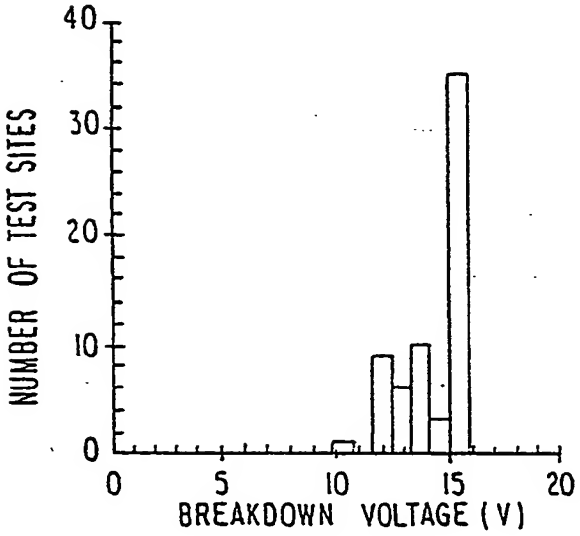


FIG. 4C
LOT # 2, 1ST PASS

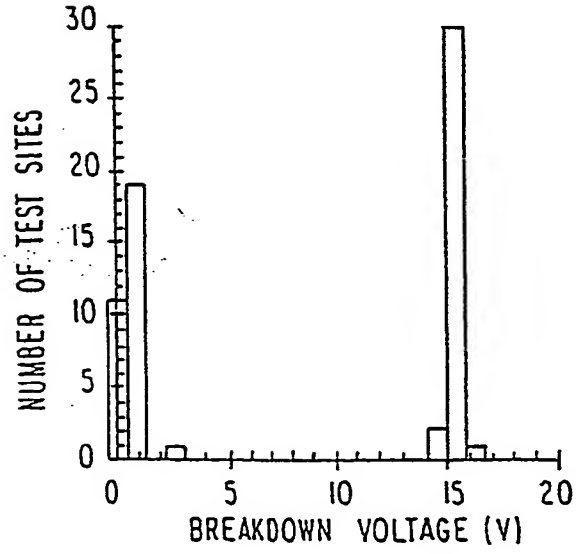


FIG. 4D
LOT # 2, 2ND PASS

FIG. 5A
LOT #1, 1ST PASS

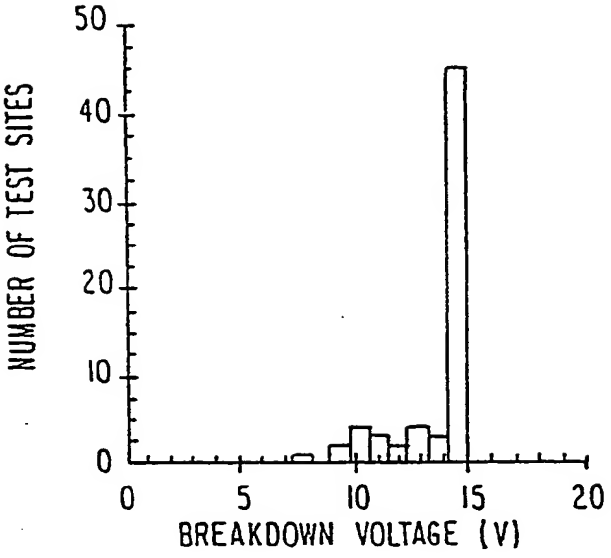
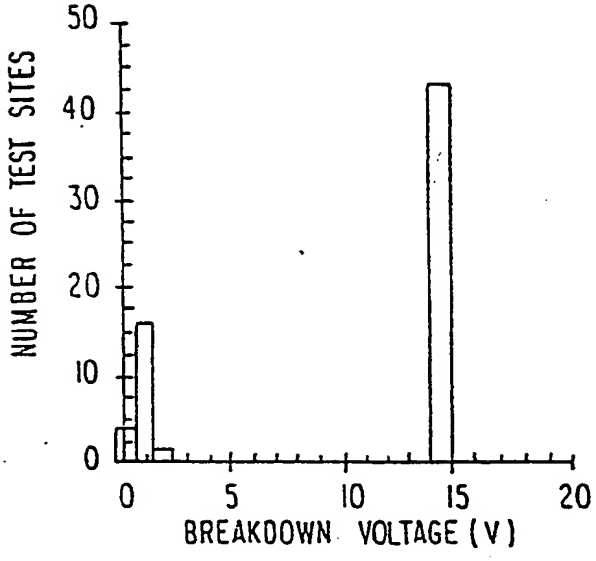


FIG. 5B
LOT # 1, 2ND PASS



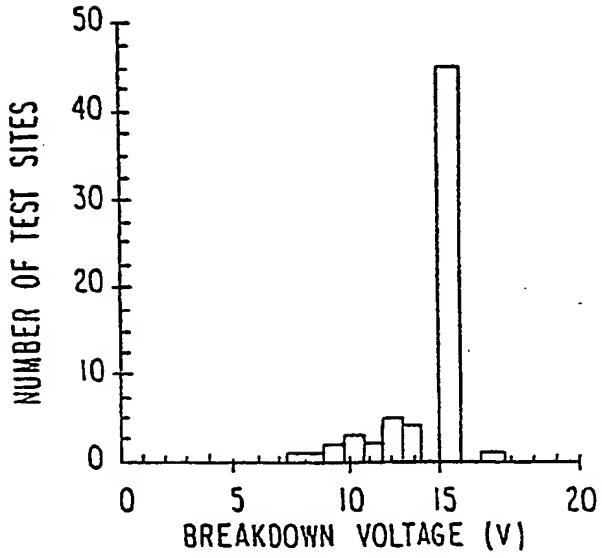


FIG. 5C
LOT # 2, 1ST PASS

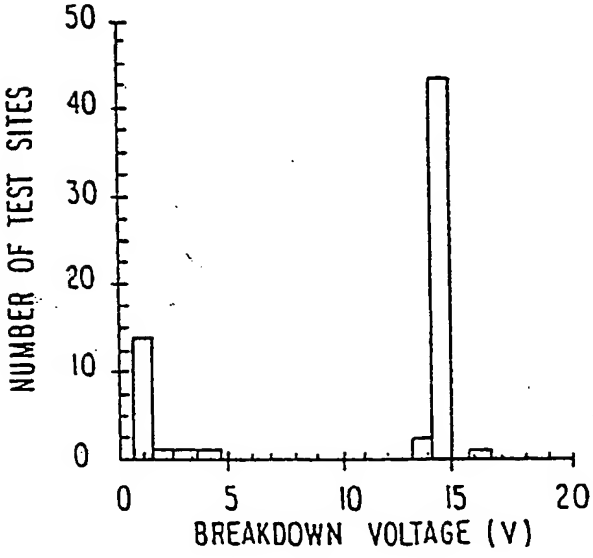


FIG. 5D
LOT # 2, 2ND PASS

FIG.6A
LOT #1, 1ST PASS

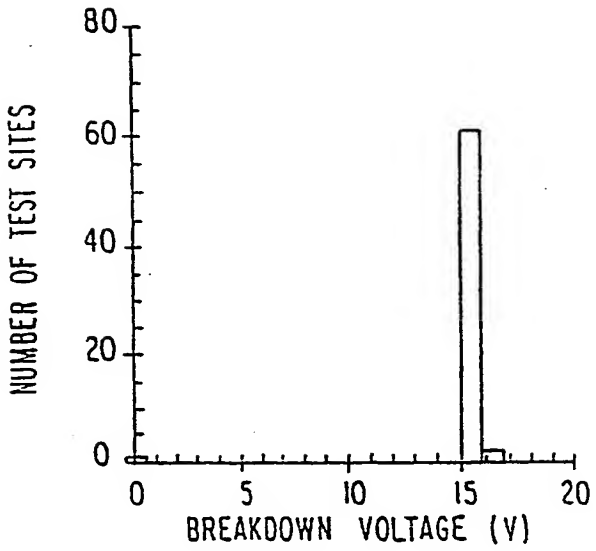
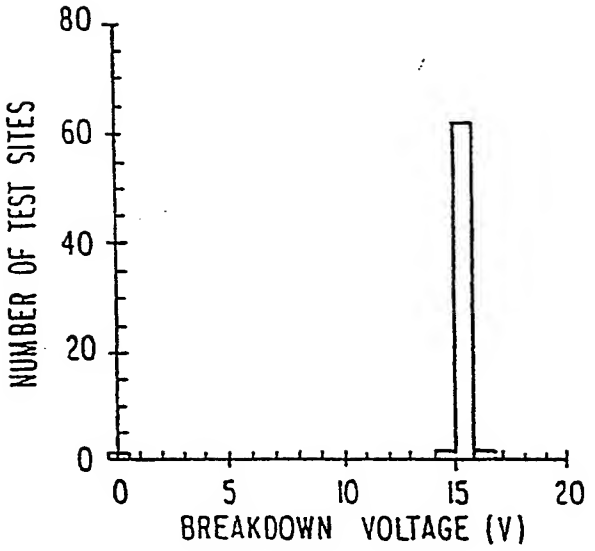


FIG.6B
LOT #1, 2ND PASS



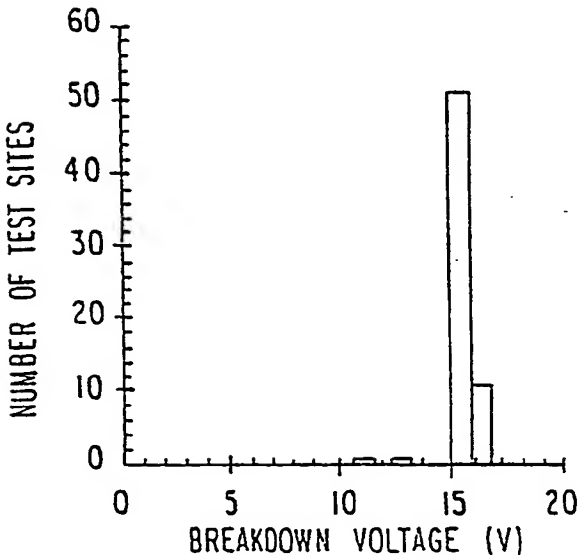


FIG.6C
LOT # 2, 1ST PASS

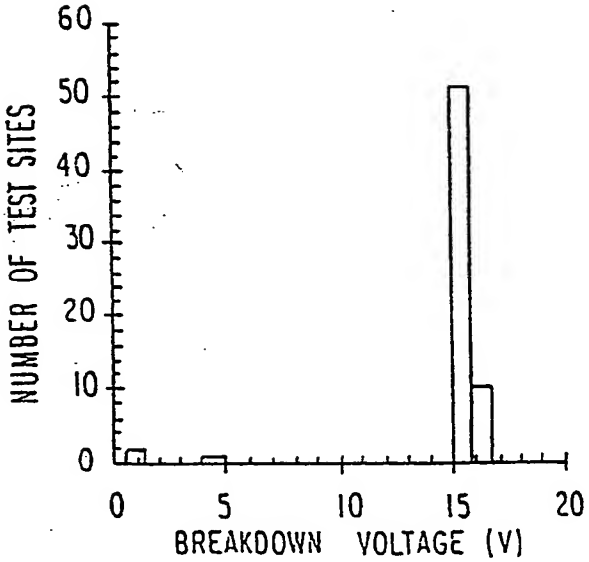


FIG.6D
LOT # 2, 2ND PASS

FIG.7A
LOT #1, 1ST PASS

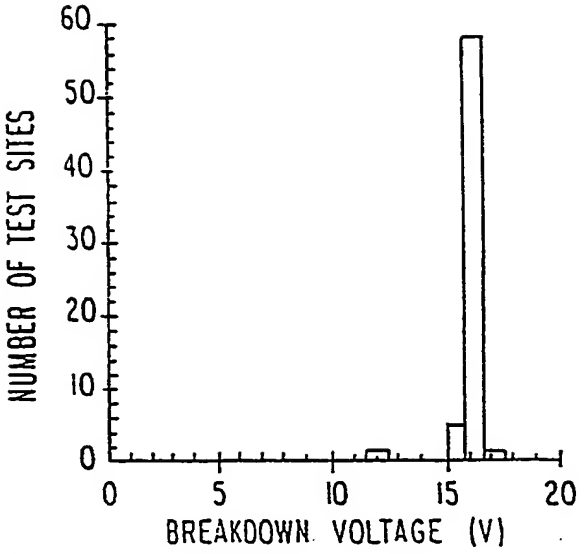
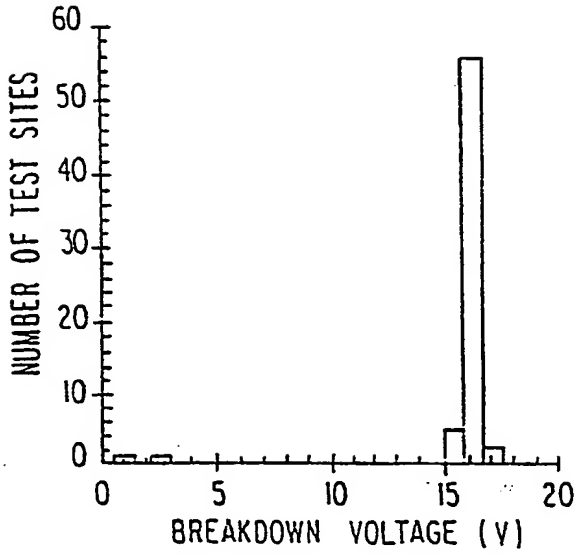


FIG.7B
LOT #1, 2ND PASS



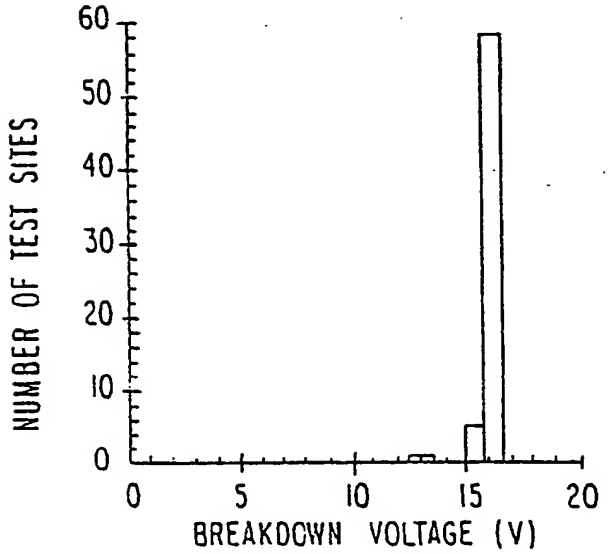


FIG.7C
LOT #2, 1ST PASS

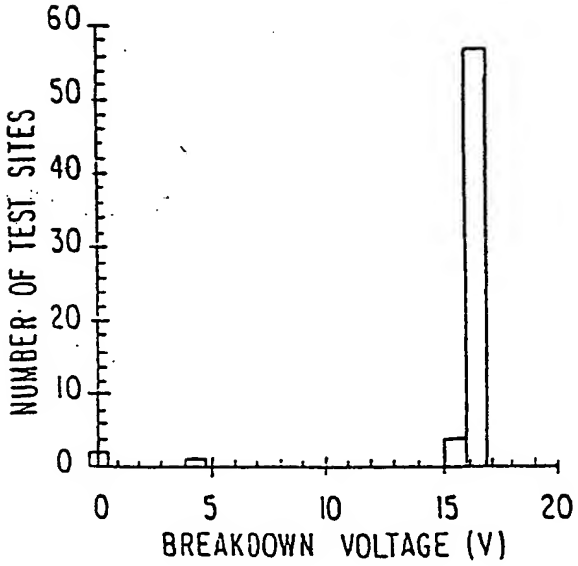


FIG.7D
LOT #2, 2ND PASS

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	WO-A-8 201 619 (HUGHES AIRCRAFT CO.) * Figures 1,2; page 9, lines 7-19; claims 1,2,11,13 * ---	1-3,11	H 01 L 21/265 H 01 L 21/314
A	US-A-4 438 157 (ROMANO-MORAN) * Abstract * ---	2,3	
A	JAPANESE JOURNAL OF APPLIED PHYSICS, vol. 19, suppl. 19-1, 1980, pages 61-64, Tokyo, JP; K. YAGI et al.: "Low-frequency low-noise transistors fabricated by double ion implantation" * Page 61, column 1, lines 24-29; page 61, column 2, lines 5-17; page 62, table 1; figure 1 * ---	1-3,7	
A	JOURNAL OF APPLIED PHYSICS, vol. 58, no. 12, December 1985, pages 4633-4637, American Institute of Physics, Woodbury, New York, US; A. FAIGON et al.: "Trapping effects in thin oxynitride layers in metal-insulator-semiconductor devices" * Pages 4633,4634, "Experiment" * ---	1-3,8, 10,11	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L
A	IEEE ELECTRON DEVICE LETTERS, vol. EDL-6, no. 1, January 1985, pages 3-5, New York, US; M. SEVERI et al.: "Effect of thermally nitrided SiO2 thickness on MIS characteristics" * Page 3, column 1, line 32 - column 2, line 10; page 5, lines 4-11 * --- -/-	4,6,11	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13-11-1987	GELEBART Y.C.M.

CATEGORY OF CITED DOCUMENTS

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L : document cited for other reasons

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Application Number

EP 87 11 2149

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
D,A	JOURNAL OF ELECTRONIC MATERIALS, vol. 14, no. 5, September 1985, pages 617-632, The Metallurgical Society of AIME; P. PAN et al.: "Properties of thin LPCVD silicon oxynitride films" * Pages 619,620: "Experimental"; page 625, line 19; figure 7 *	1-5,7, 11	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13-11-1987	GELEBART Y.C.M.

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